IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: METHOD, CHEMISTRY, AND APPARATUS FOR NOBLE METAL ELECTROPLATING ON A MICROELECTRONIC WORKPIECE

Application No.: 09/429,446 Group No.: 1741

Filed: October 28, 1999 Examiner: W.T. Leader

Inventors: L.W. Graham et al.

COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

DECLARATION OF PRIOR INVENTION IN THE UNITED STATES TO OVERCOME CITED PATENTS OR PUBLICATIONS (37 C.F.R. § 1.131)

1. This declaration is to establish completion of our invention as described and claimed in this application in the United States prior to July 22, 1998, which is a date prior to the effective date of U.S. Patent Nos. 6,132,587 to Jorné et al., 6,074,544 to Reid et al., 6,140,241 to Shue et al., 6,077,412 to Ting et al., 6,107,186 to Erb, and 6,203,684 to Taylor, et al., that were each cited by the Examiner in this application.

2. We, the persons making this declaration, are the inventors of the subject matter described and claimed in this application.

3. To establish the date of completion of the invention described and claimed in this application, the following attached documents are submitted as evidence that we completed our invention as described and claimed in the subject application in the United States prior to July 22, 1998:

a. In laboratories at Semitool, Inc. in Kalispell, Montana, prior to July 22, 1998, a series of tests to electroplate a noble metal onto a patterned semiconductor wafer were conducted. These tests are described on pages 29-38 from the co-inventor, Lyndon Graham's notebook attached hereto as Exhibit A. During the tests described in Exhibit A, an electroplating solution containing platinum, a noble metal ion was used, see page 29. The patterned semiconductor wafer was contacted with the electroplating solution through adjustment of the head supporting the wafer, see page 29. The surface of the semiconductor wafer included a seed layer of no more than 1,000 angstroms thick, see page 32. The summary of results on page 38 describes that wafers 19 and 20 (used in run 5 and run 6, described on page 32), are patterned. The tests employed an initial low current electroplating power for a first period of time followed by applying a higher current electroplating power for a second period of time, see page 30. The electroplating power was halted and the wafers removed from the electroplating solution prior to the visual inspection of the wafers, the results of which are set forth on pages 37 and 38.

b. Each of the dates blacked out from pages 29-38 of Exhibit A is prior to July 22, 1998.

4. The pages of Exhibit A evidence that our invention, as described and claimed in this application, was completed prior to July 22, 1998.

5. This declaration is submitted as the required submission in conjunction with the filing of a Request for Continued Examination.

6. As a person signing below:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Inventors

Full name of **first** inventor: Lyndon W. Graham
Inventor's signature: Lyndon W Graham
Date: 3/6/03
Residence: Country of Citizenship: U.S.A.
Post Office Address: 1937 S.E. Morgan Road, Hillsboro, OR 97123
Same as above.

Full name of **second** inventor: Curt W. Jacobson
Inventor's signature: _____
Date: _____
Residence: Country of Citizenship: U.S.A.
Post Office Address: 520 6th Avenue East, Kalispell, MT 59901
Same as above.

Full name of **third** inventor: Thomas L. Ritzdorf
Inventor's signature: _____
Date: _____
Residence: Country of Citizenship: U.S.A.
Post Office Address: 3130 Parkwood, Bigfork, MT 59911
Same as above.

JMS:jas/mk